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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/838,074	04/19/2001	Mark A. Maciver	GB900051US1	9566

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 02/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,074	MACIVER, MARK A.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings filed April 19, 2001 are accepted.

Specification

The disclosure filed April 19, 2001 is accepted.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "substantially" in line 6 of claim 7 creates ambiguity and is a relative term and therefore should be removed form claim language. The Examiner would like to point out that claims 8-12 depend from independent claim 7 and inherently include limitations therein and therefore are rejected for reason stated above.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Byers et al. (USPN 5784393).

As per claims 1 and 7, Byers et al. (herein after: Byers) substantially teaches (title and abstract) a method and apparatus for providing fault detection to a corresponding bus when one or more of the users connected to the bus does not have a fault detection capability provided therein. Furthermore, Byers teaches a method and apparatus for performing fault detection on a corresponding bus when the width of the bus is insufficient to accommodate a number of parity bits. In an exemplary embodiment, a selected one of the number of users may validate all bus transmissions via a number of transceivers, regardless of which user has a fault detection capability provided therein. In another exemplary embodiment of the present invention, a transmitting user may provide a data word and a number of corresponding parity bits. The transmitting user may provide the data word to the bus while storing the corresponding number of parity bits therein. The data word may be provided back to the transmitting user via the corresponding transceivers wherein the transmitting user may check the data word against the

number of parity bits previously generated by the transmitting user. In particular, Byers teaches (Figure 3) a first portion and a second portion of a data processing system that transmits a data word with corresponding parity bits. In the second portion Byres teaches to test and detect errors in the received information via the parity checker.

Byers does not explicitly teach a parity generator in the first portion as stated in the present application.

However, Byers teaches (col. 1, lines 44-59) that typical system which uses parity as an error detection mechanism has a *parity generation circuit* for generating the parity bit. For example, when the system stores a data word into a memory, the parity generation circuit generates a parity bit from the data word and the system stores both the data word and the corresponding parity bit into an address location in the memory. When the system reads the address location where the data word is stored, both the data word and the corresponding parity bit are read from the memory. The parity generation circuit then regenerates the parity bit from the data bits read from the memory device and compares the regenerated parity bit with the parity bit that is stored in memory. If the regenerated parity bit and the original parity bit do not compare, an error is detected and the system is notified. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate a parity generator at the first portion of the data processing system as stated in the present application. This modification would have been obvious to one of ordinary skill because one of ordinary skill would have recognized that a parity generator is essential in generating parity and it would have been convenient for a designer to place at the first portion of the data processing system.

As per claims 2 and 8, Byers substantially teaches, in view of above rejection, a connector as stated in the present application. The Examiner would like to point out that for all practical purposes an interface is a connector. An interface is defined as *a surface forming a common boundary between adjacent regions, bodies, substances, or phases.* A connector is defined as *something that joins or links together.* Furthermore, Byers teaches (abstract) a method and apparatus for providing fault detection to a corresponding bus when one or more of the users are **connected** to the bus.

As per claims 3 and 7, Byers substantially teaches, in view of above rejection, (Figure 6) is a schematic diagram of an exemplary embodiment of the host interface adapter block. For illustration, Host Interface Adapter (HIA) 534 of FIG. 5 is shown. It is recognized that HIA 544 may be similarly constructed. HIA 534 may comprise two Microsequencer Bus Controllers (USBC) 640, 642 which may be connected to a control store 644 via interface 646. The USBC's 640, 642 may access the HIA stations 628, 622, 618, and 636 via a microbus 638. A player+0 602 and a player+1 600 may receive frames (or data elements) over fiber optic link 530. The term player+ refers to a fiber optic interface controller available from National Semiconductor which is called the Player Plus Chip Set. Player+0 602 may forward its frame to light pipe control 604 via interface 606. Similarly, player+1 600 may forward its frame to light pipe control 604 via interface 606. Light pipe control 604 may transfer the frames to a Receive Frame Transfer Facility (REC FXFA) 608 via interface 610. REC FXFA 608 may unpack the frames and may store control information in a Request Status Control Table-0 (RSCT-0) 628 and a RSCT-1 622 via interface 620. RSCT-0 628 and RSCT-1 622 may monitor the data that has been received from a corresponding data mover. The data which was contained in the frame

received by REC FXFA 608 may be sent to the Database Interface (DBIF) station 618 via interface 620. DBIF 618 may forward the data over interface 632 to the streets.

As per claims 4-6 and 10-12, Byers substantially teaches, in view of above rejection, (col. 22, lines 1-25) an error detection logic block 874 may be coupled to address input register 864 via interface 868. Error detection logic block 874 may comprise a SRAM address register 872. SRAM address register 872 may capture an SRAM address when an SRAM read error is detected. That is, SRAM address register 872 may store the read address that is present on DSD address bus 650 in response to an SRAM read error. Error detection block 874 may monitor the data that is present in DSD bus 650 via interface 754. Error detection block 874 may thus perform a parity check or the like on the data presently read from memory 680. If an error exists, error detection block 874 may enable SRAM address register thereby capturing the current read address. This may identify the faulty read address within memory 680. Error correction block 874 may then provide the faulty read address to USBC0 640 for further processing via interface 820. For example, USBC0 640 may read and write various test patterns to the faulty read address to determine if the fault was caused by a soft error or a hard error. If the fault was caused by a soft error, the contents of memory 680 may be reloaded and the operation of the computer system may continue. However, if the fault was caused by a hard error, the operation of the computer system may be interrupted. Other error detection schemes are contemplated and may be incorporated into error detection block 874.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Byers substantially teaches a method and apparatus for providing error detection and correction in an interface between two portions of a data processing system. Applicant is invited to read/review additional pertinent prior art has been included herein with this office action. IDS has been considered and the PTO-1449 form is attached hereto.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
February 15, 2004

Guy J. Lamarre
for

Albert DeCady
Primary Examiner